

RESEARCH ARTICLE

An efficient full adder circuit design in Quantum-dot Cellular Automata technology

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Abstract: Quantum-dot Cellular Automata (QCA) is potentially a very attractive alternative to CMOS for future digital designs. Circuit designs in QCA have been extensively studied. QCA technology has been extensively investigated in recent years. However, only limited attention has been paid to QCA decimal arithmetic. In this paper, an efficient full adder is presented. The layout of the proposed circuit uses 30 QCA cells and a 25% improvement over the best previous design. It has significant improvements in comparison to the previous designs in terms of the number of cells, area and cost and has a similar delay to the fastest previous design. In Ripple Carry Adder (RCA) design, they also maintain high performance. And all of the multi-bit RCA also have the lowest overall cost with a reduction of over 50% when compared with the previous RCA design.

Keywords: full adder, nanotechnology, quantum-dot cellular automata, ripple carry adder

1 Introduction

The current Complementary Metal Oxide Semiconductor (CMOS) technology has almost reached its physical scaling limitation. The reduction of CMOS technology brings severe challenges in terms of physical dimensions, power consumption and leakage current. In the future development of integrated circuit technology, nanoelectronics technology has been widely studied for its novel properties. Quantum-dot Cellular Automaton (QCA) technology is a potential alternative to CMOS technology^[1]. Unlike traditional circuits, as for this technique, the logic states are encoded based on the position of the electrons. Therefore, it not only provides a nano-level solution method, provides a new paradigm for information transmission, calculation and exchange, but also has the advantages of fast switching speed, low power consumption, and high density^[2].

QCA cell is the smallest unit of QCA technology. It is a tiny nanoscale-building block for computing and signal processing. QCA cells communicate with each other through Coulomb repulsion on a large array using electron permutation of quantum-dots in cells^[3]. This fea-

ture would make this paradigm radically different from the existing current-switching transistors. QCA technology used a smart information encoding mechanism suitable for nanostructures, eliminating the problems of the current-switching transistors. The QCA cell array contains the information based on electrons charges polarization arrangement and does not include the transport of charges. In other word, the interaction between QCA cells and neighboring cells is directly generate the dynamic and stable to one of two ground states (i.e. logic '0' and logic '1'). In the QCA circuit, the timing, calibration, and recovery of signals are controlled by an external clock and operated according to the rules of Boolean logic^[4].

QCA technology provides a revolutionary approach to computing and opens up a new pattern for circuit design. The most important operations in computer systems such as multiplication, subtraction, and division are based on simple modifications of the full adder circuit. Therefore, it can be seen that in computers, information processing and operations, the full adder is the basic and key element. So, an efficient adder structure is the key to designing a high-performance arithmetic circuit. The high-performance full adder circuit design has also attracted much attention. Therefore, many researchers have designed full adder circuits to improve the efficiency of full adder circuits in QCA technology. In this paper, we propose an efficient QCA full adder structure. Compared with the adder design structure in other previous literatures, it has been greatly improved based on a comprehensive consideration of some QCA circuit's met-

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rics. In addition, to verify that our proposed full adder structure has good scalability, 4-, 8-, and 16-bit Ripple Carry Adder (RCA) circuits were also implemented in this work.

In this paper, we propose an efficient full adder circuit in QCA. Compare to other QCA based full adder design, the number of the QCA cells is few, layout area of the circuit is small, the time delay from input cell to output cell of this circuit is short, and the value of cost is low. The rest of this paper is organized as follows. Section 2 briefly introduces the background of QCA technology. Section 3 reviews the logical relationship between input and output about a full adder, as well as several previous typical QCA adder circuit structures. An efficient structure of 1-bit full adder is demonstrated and the 4-, 8-, and 16-bit RCA designs are implemented by using the proposed full adder in section 4. Section 5 illustrates the simulation results for the proposed full adder, as well as the comparison results of the full adder design and the RCA design with previous better designs. And finally, conclude our paper in Section 6.

2 QCA technology

2.1 Fundamental QCA components and logic gates

The basic element in QCA technology is a QCA cell, which is a nanoscale square structure with two electrons and four quantum dots. According to coulomb repulsion, two electrons must be located on the antipodal site of the cell in ground states. If the potential barrier between quantum dots is reduced by a certain value, the electrons in the cell can arbitrarily tunnel between the quantum-dots. It's important to note that the tunnelling effect occurs only within the cell. Therefore, there are two stable charge configurations in the QCA cell representing two polarization states. These two states can be used to encode binary information, the polarizations '-1' and '+1' represent the binary logic values '0' and '1', respectively. Figure 1(a) and 1(b) show two types of QCA cells, called normal cells and rotated cells, respectively. Rotated cells are usually used for coplanar crossings. A QCA Wire is created by placing a series of cells side by side. As shown in Figure 1(c), the QCA wire includes an input cell, an output cell and some free cells. Due to Coulomb interactions, the value of a logical '0' or '1' from the input cell will be transfer through the chain of free cells^[5].

In the traditional digital circuit design, the basic logic gates includes AND gate, OR gate and NOT gate. Similarly, the base logic gates in QCA are inverter and 3-

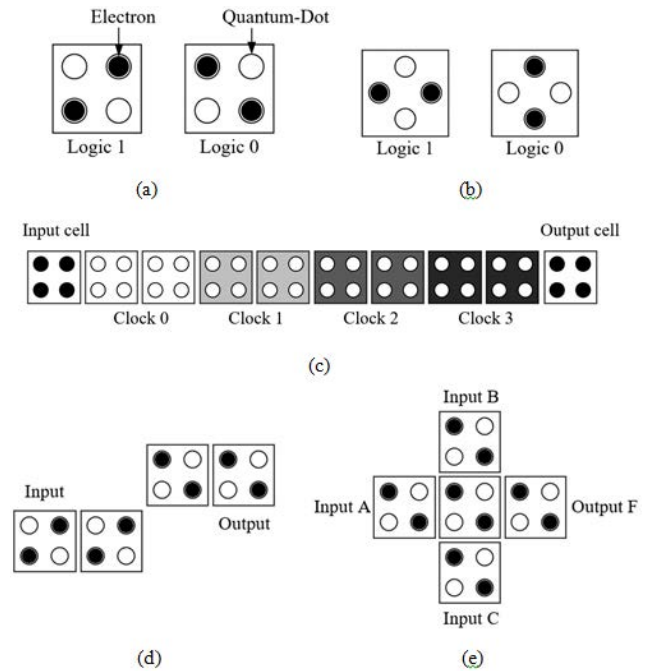


Figure 1. QCA logic and fundamental QCA components: (a) normal cell; (b) rotated cell; (c) QCA wire; (d) Inverter gate; (e) 3-input majority gate

input majority gate. Inverter is usually constructed by positioning two cells diagonally from each other. In QCA technology, inverter can be included in the interconnected wire because it does not create any additional latency. Figure 1(d) shows a schematic diagram of the inverter gate. A structure of 3-input majority gate is more complicated than the inverter's. The schematic of the 3-input majority gate is shown in Figure 1(e), which demonstrates it consists of five QCA cells, shaped like a cross. If any two or three input values of the 3-input majority gate are '1', the output value of the 3-input majority gate is '1', and in other cases the output value is '0'. Obviously, theoretically setting any one input of the 3-input majority gates to '0' will change the 3-input majority gate into a 2-input AND logic gate. Similarly, setting any one input of the 3-input majority gates to '1' will change the 3-input majority gate into a 2-input OR logic gate. Therefore, the Boolean logic expression of the 3-input majority gate can be expressed as

$$F = AB + BC + AC \quad (1)$$

In QCA technology, all logic functions can be implemented by the combination of inverter and the 3-input majority logic gate^[5].

With the development of QCA technology, a majority logic gate with five inputs was created. The design and implementation of the 5-input majority gate based on QCA technology has been explored in work such as

Ref. [6]^[6]. Five-input majority gates work the same way as three-input majority gates, if any three or more of the 5-input values in the 5-input majority gate are ‘1’, the output of the 5-input majority logic gate is ‘1’, otherwise it is ‘0’. Similarly, the output of a 5-input majority gate expression is

$$F = ABC + ABD + ABE + ACD + ACE + ADE + BCD + BCE + BDE + CDE + AC \quad (2)$$

2.2 QCA clocking scheme

Four-phase clocking in each QCA clocking zone is typically used. There is a 90° phase shift from one clocking zone to the next, which is shown in Figure 2. The clock signals of QCA circuits are generated by an electric field applied to the QCA cells to modulate the tunnelling barrier between dots. The transition and conversion of information takes place in the ‘SWITCH’ phase. A cell is latched during the ‘HOLD’ phase. A clocked QCA ‘wire’ can be considered as a chain of D-latches. The smallest unit of delay in QCA is a clocking zone delay (latency) which is the quarter of the clock cycle delay.

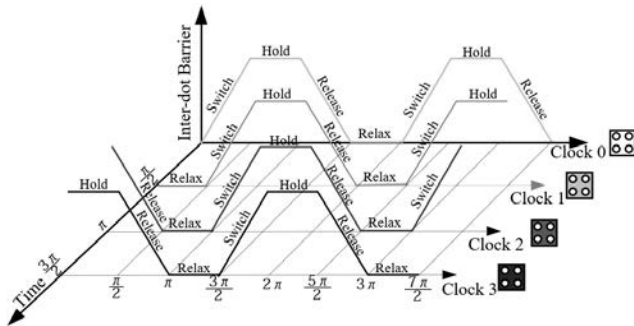


Figure 2. Clocking scheme

2.3 QCA Wire Crossings

Because of the interaction of adjacent cells, the input data is carried down arrays of the QCA cells. Binary data is transferred from one physical location to another by wire. In general, there are two types of wire crossing, which that is multilayer crossover and coplanar crossover. As shown in Figure 3(a), a coplanar crossing is proposed^[7] as a unique property of a QCA layout that uses only one layer for the crossover. A coplanar crossover uses both normal cells and rotated cells, which they do not interact with each other when they are properly aligned. The other option is multilayer crossover^[8], which uses a minimum of three layer and used more cells. It similar to the placement and routing of metal

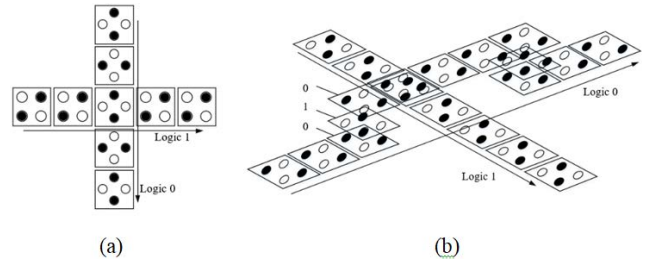


Figure 3. QCA crossover: (a) coplanar crossover; (b) multilayer crossover

wires in CMOS technology as shown in Figure 3(b). According to coulomb repulsion, the polarization of stacked cells becomes inverse when the value is passing between layers. So, the multi-layer crossover needs at least three layers to achieve.

3 Overview of full adder in QCA

To design a full adder, we need a formulation for sum output of full adder. In a full adder, carry and sum are defined as Equation (3) and (4).

$$C_o = A_i + B_i + C_i = MAJ3(A_i, B_i, C_i) \quad (3)$$

$$Sum_i = A_i \bar{B}_i \bar{C}_i + \bar{A}_i B_i \bar{C}_i + C_i \bar{A}_i \bar{B}_i + A_i B_i C_i \quad (4)$$

From the Equation (3), we can know that the carry output of the full adder is generated by a three-input majority gate. Since the majority gate is the basic gate in QCA technology, carry output is optimum. In general, some researchers have to minimize the Sum_i equation in terms of the majority gates.

By using the QCA basic gate, the Equation (4) was written as

$$Sum_i = MAJ(MAJ(\bar{A}_i, B_i, C_i), MAJ(\bar{B}_i, A_i, C_i), MAJ(\bar{C}_i, B_i, C_i)) \quad (5)$$

The first full adder in QCA technology was proposed in Ref. [7]^[7] base on Equation (3) and (5), as shown in Figure 4(a). The layout of this design used 192 cells and it was implemented in a single layer. It means that the full adder is composed of five majority gates and three inverters.

By changing the Equation (4), we can show that the output of Sum_i can be generated by Equation (6-8).

$$Sum_i = MAJ3(\bar{C}_o, A_i, MAJ3(\bar{C}_o, B_i, C_i)) \quad (6)$$

$$Sum_i = MAJ3(\bar{C}_o, B_i, MAJ3(\bar{C}_o, A_i, C_i)) \quad (7)$$

$$Sum_i = MAJ3(\bar{C}_o, C_i, MAJ3(\bar{C}_o, B_i, A_i)) \quad (8)$$

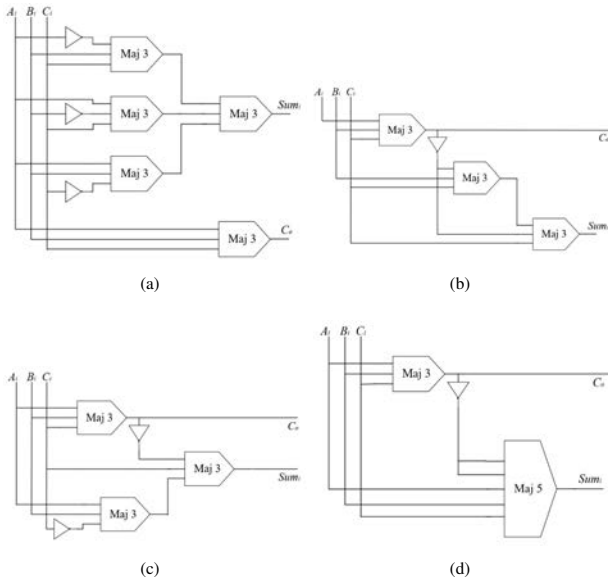


Figure 4. The structure of 1-bit full adder in, (a)^[7], (b)^[8], (c)^[5], (d)^[9]

According to the Equation (8), as demonstrated in Figure 4(b), another design of full adder consists of three majority gates and one inverters in Ref. [8]^[8]. The QCA layouts of this design has 0.75 clock cycles latency and uses 38 cells.

We can also obtain the Equation (9) by rewriting the Equation (2).

$$\text{Sum}_i = \text{MAJ3}(\bar{C}_o, C_i, \text{MAJ3}(A_i, B_i, \bar{C}_i), C_i) \quad (9)$$

Figure 4(c) shows the schematic diagram of the Equation (9), uses three 3-input majority gates and two inverters.

In addition, the Equation (4) can also be rewritten by using a five-input majority gate with the value of the output C_o of the full adder also being used as an input. The equation for Sum then becomes:

$$\text{Sum}_i = \text{MAJ5}(A_i, B_i, C_i, \bar{C}_o, \bar{C}_i) \quad (10)$$

According to the Equation (10), a design of full adder was proposed in Ref. [9]^[9]. As shown in Figure 4(d), this design consist of a three-input majority gate, one inverter, and an unconventional form of majority gate with five inputs.

4 Proposed QCA full adder

In this paper, according to the principle of Equation (10), we propose an optimized full adder circuit design based on the structure of Figure 4(d). All along, some researchers have presented some optimization designs

based on Equation (10). For example, as described in Ref. [10]^[10], and it seems not to be a significant improvement, our proposed full adder is much simpler than previous designs.

The QCA layout of the proposed 1-bit full adder is shown in Figure 5. A_i , B_i , and C_i are the inputs of the proposed full adder, while C_o and Sum_i are the outputs of the proposed full adder. It consists of three logic gates, which are an inverters, a 3-input majority and a 5-input majority gate. Figure 5 shows a QCA-based implementation of 1-bit full adder circuit with only 30 cells and without using any irregular cells. The full adder design has only 0.75 clock cycles of latency, and its circuit occupies a small area, only $0.01 \mu\text{m}^2$. Figure 6 displays three different layers of the proposed full adder.

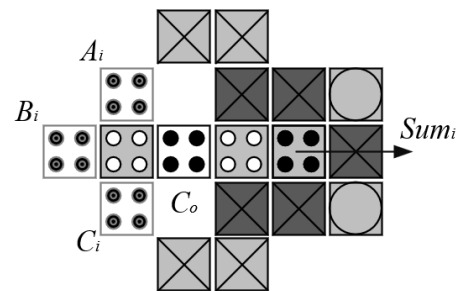


Figure 5. Layout of the proposed QCA full adder

In order to prove that the optimized full adder has good scalability and superiority in terms of cell count, circuit area, latency, and the cost of QCA, the 4-, 8-, and 16-bit RCAs based on QCA were also implemented. As we know, the working principle of RCA circuit is very simple. Several full adders can be easily connected in series to achieve RCA circuit. The output carry of the adjacent low full adder is used as the carry input of the adder.

For example, a 4-bit RCA is composed of 4 1-bit full adders. The inputs to be added are defined as A_3, A_2, A_1, A_0 and B_3, B_2, B_1, B_0 , and their sum is defined as S_3, S_2, S_1, S_0 . The layout of the 4-bit RCA is shown in Figure 7(a). This design uses 144 normal QCA cells, the circuit occupies an area of $0.13 \mu\text{m}^2$, the delay value from input to output is 1.5 clock cycle, and the value of cost function is 0.2925.

Figure 7(b) shows the layout of 8-bit RCA. The design uses 398 normal QCA cells, the circuit occupies an area of $0.43 \mu\text{m}^2$, the delay value from input to output is 2.5 clock cycle, and the value of cost function is 2.6875.

Figure 7(c) illustrates the layout of 16-bit RCA. The design uses 1043 normal QCA cells, the circuit occupies an area of $1.47 \mu\text{m}^2$, the delay value from input to output is 4.5 clock cycle, and the value of cost function is

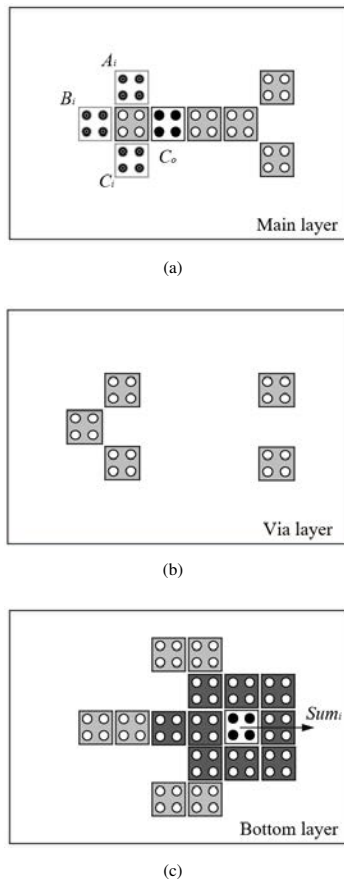


Figure 6. Three different layers of the proposed QCA full adder

29.7675.

5 Simulation and experimental results

In this paper, the proposed full adder is implemented and simulated by using QCA Designer software with the coherence vector simulation engine setup, and all of the mentioned parameters are default values in QCA Designer software.

Table 1 gives the mentioned parameter values used in the simulation mode.

From the Figure 8, we can know, when the input value is ‘100’, the output Sum_i is ‘1’ and C_o is ‘0’. When the input value is applied after a 0.75 clock cycle’s latency, the output appears. The results confirm that the proposed full adder work properly and exactly like the function of a full adder.

Table 2 which compares the designs of full adders proposed in previous works and this letter based on some important metrics, it shown that our proposed design is better in all metrics than previous designs. As is demonstrated, our proposed design uses only 30 QCA cells whereas the existing best design^[8] used 38 QCA

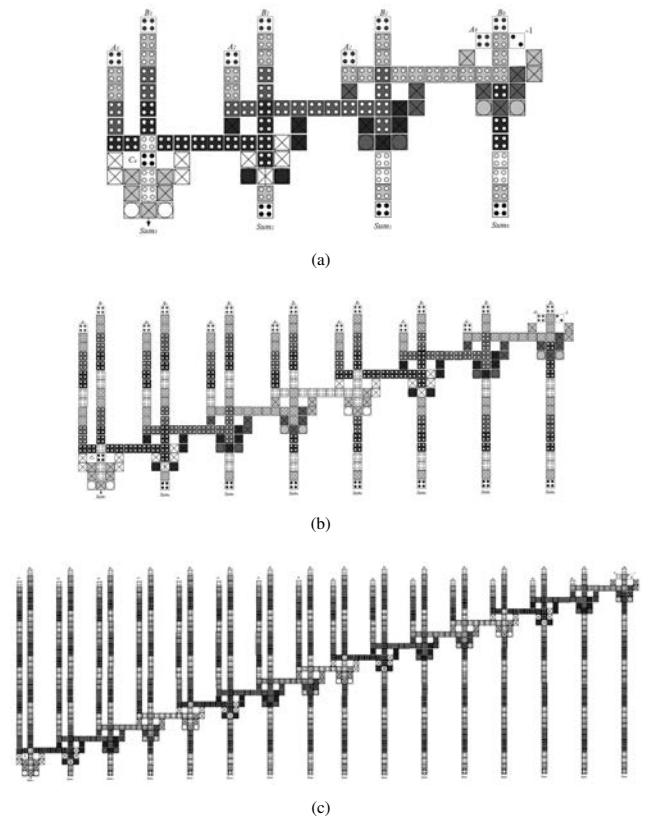


Figure 7. The layout of ripple carry adder, (a) 4-bit, (b) 8-bit, (c)16-bit

cells which mean about 25 percent improvement. In our proposed design circuit, the layout area is also reduced greatly, with a design area of $0.01\mu m^2$, whereas two better designs proposed in Ref. [11]^[11] and Ref. [8]^[8], were $0.03\mu m^2$ and $0.02\mu m^2$ which means reduce by 66 and 50 percent, respectively. And the design’s area in Ref. [13]^[13] is $0.1\mu m^2$ which means that our design’s area is one-tenth of its. The latency of our proposed design is 0.75 which has a similar delay to that of the fastest designs previously. The Cost of circuit, which evaluated the QCA circuit, the value of cost depended on the area and delay. In our proposed design, the cost is 0.005625, which means the value much smaller than the previous designs. The comparison results are shown that the full adder design we proposed is the most optimal full adder.

Table 3 summarizes the characteristics of ripple carry adder designs of various bit in some better previous design in Ref. [8],^[8] Ref. [11]^[11] and the design in this paper.

According to Table 3, comparison of RAC in terms of the number of cells. The proposed 4-bit RCA uses only 144 cells, whereas the design in Ref. [8]^[8] and Ref. [11]^[11] used 237 cells and 308 cells which mean about 39 and 53 percent improvement, respectively. The pro-

Table 1. The simulation mode’s parameters

| Parameter | Value |
|---------------------------|---------|
| Cell width (nm) | 18.0 |
| Cell height (nm) | 18.0 |
| Quantum-dot diameter (nm) | 5.0 |
| Relaxation time (s) | 1.0E-15 |
| Time-step (s) | 1.0E-16 |
| Total simulation time (s) | 7.0E-11 |
| Clock-high (Joule) | 9.8E-22 |
| Clock-low (Joule) | 3.8E-03 |
| Clock amplitude factor | 2.0 |
| Radius of effect (nm) | 80.0 |
| Relative permittivity | 12.9 |
| Layer separation (nm) | 11.5 |

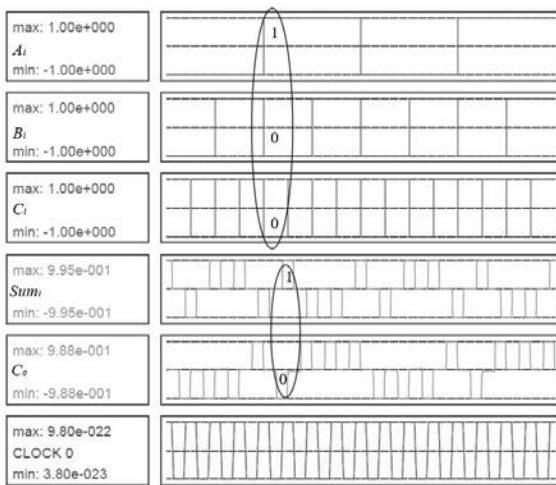


Figure 8. Simulation results for the full adder circuit

Table 2. Comparison of the full adder designs

| Design | Cells | Area (μm^2) | Latency | Cost |
|-----------|-------|--------------------|---------|----------|
| Ref. [6] | 61 | 0.03 | 0.75 | 0.016875 |
| Ref. [8] | 38 | 0.02 | 0.75 | 0.011250 |
| Ref. [10] | 63 | 0.05 | 0.75 | 0.028125 |
| Ref. [11] | 51 | 0.03 | 0.75 | 0.016875 |
| Ref. [12] | 73 | 0.04 | 0.75 | 0.022500 |
| Ref. [13] | 86 | 0.1 | 0.75 | 0.056250 |
| Proposed | 30 | 0.01 | 0.75 | 0.005625 |

Table 3. Summary of ripple carry adders (RCA) designs for various bit length

| Design | Bits | Cells | Area (μm^2) | Latency | Cost |
|-----------|------|-------|--------------------|---------|-----------|
| Ref. [8] | 1 | 38 | 0.02 | 0.75 | 0.011250 |
| | 4 | 237 | 0.24 | 1.50 | 0.540000 |
| | 8 | 517 | 0.59 | 2.50 | 3.687500 |
| | 16 | 1224 | 1.55 | 4.50 | 31.387500 |
| Ref. [11] | 1 | 51 | 0.03 | 0.75 | 0.016875 |
| | 4 | 308 | 0.29 | 2.00 | 1.160000 |
| | 8 | 695 | 0.79 | 3.75 | 11.109375 |
| | 16 | 1759 | 2.51 | 5.00 | 62.750000 |
| Proposed | 1 | 30 | 0.01 | 0.75 | 0.005625 |
| | 4 | 144 | 0.13 | 1.50 | 0.292500 |
| | 8 | 398 | 0.43 | 2.50 | 2.687500 |
| | 16 | 1043 | 1.47 | 4.50 | 29.767500 |

posed 8-bit RCA uses only 398 cells, whereas the design in Ref. [8]^[8] and Ref. [11]^[11] used 517 cells and 695 which mean about 23 and 42.7 percent improvement, respectively. The proposed 16-bit RCA uses 1043 cells, whereas the design in Ref. [8]^[8] and Ref. [11]^[11] used 1224 cells and 1759 which mean about 14.8 and 40.7 percent improvement, respectively. Similarly, we can know that all of the proposed RCA occupy less area than design in Ref. [8]^[8] and Ref. [11]^[11]. The proposed RCAs has smaller latency than the designs in Ref. [11]^[11], and has lower cost than the design in Ref. [8]^[8] and Ref. [11]^[11].

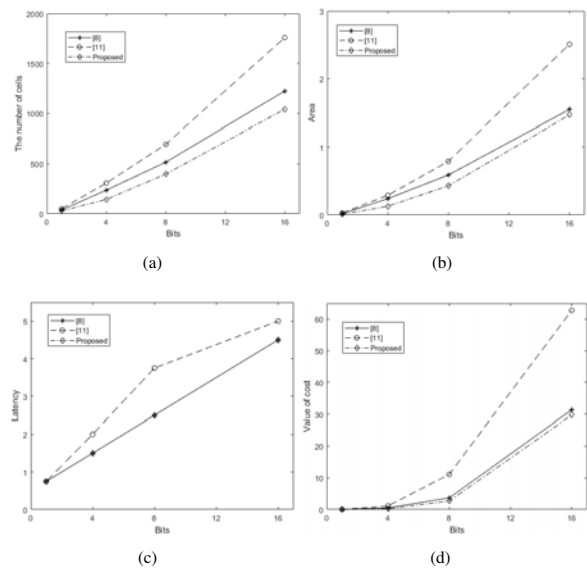


Figure 9. Comparison of, (a) the number of cells, (b) area, (c) latency, (d) value of cost

The proposed adders has several improvements over any of the other full adders in any metrics. Several adders mentioned in the paper and the adders designed in this paper are compared according to the number of cells, area, latency and cost.

The comparison results in term of the number of cells, area, latency and cost are shown in Figure 9(a), 9(b), 9(c) and 9(d), respectively. Obviously, it can be drawn that the ripple carry adder designs our proposed have a much smaller area, low cells, smaller latency and cost than the designs in the other literature, it is evident that our designs are better than the other designs.

6 Conclusion

In this paper, we have proposed an optimized full adder circuit design in QCA technology. The layout of the proposed circuit has merely 30 cells and a 25% improvement over the best previous design. The full

adder which we proposed, has significant improvements in comparison to the previous designs in terms of the number of cells, area and cost and has a similar delay to the fastest previous design. To evaluate the proposed QCA full adder design in larger adders, we designed the 4-bit, 8-bit and 16-bit ripple carry adders using the proposed full adder design. Our proposed designs for the full adder and ripple carry adder are preferable to the previous designs and are indeed better performance in some metrics.

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